



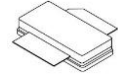
1300MHz, 250W, 28V High Power RF LDMOS FETs

Description

The ITBH13250B2 is a 250-watt, internally matched LDMOS FET, designed for multiple applications from 1000-1400MHz, especially 1300MHz RF Energy applications.

It is also qualified to operate at 32V.

ITBH13250B2



• Typical performance (on 1.3G narrow band application fixture with device soldered)

- Signal: pulse width 100us, duty cycle 10% , Vgs=2.74V, Vds=32V, Idq=120mA

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	η(%)
1300	43.5	55.9	389	1.95	12.4	66%

- Signal: CW Vgs=2.74V, Vds=32V, Idq=120mA

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	η(%)
1300	32.4	49	80	6.68	16.6	37%
1300	33.4	50.28	107	7.8	16.88	43%
1300	34.4	51.38	137	9	16.98	48%
1300	35.4	52.3	170	10.26	16.9	52%
1300	36.4	53.1	204	11.5	16.7	55%
1300	37.4	53.7	234	12.8	16.3	57%
1300	38.5	54.36	273	13.96	15.86	61%
1300	39.5	54.7	295	14.9	15.2	62%
1300	40.5	55.08	322	15.78	14.58	64%
1300	41.5	55.3	339	16.4	13.8	65%
1300	42.5	55.45	351	16.85	12.95	65%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	75	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _C	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
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Thermal Resistance, Junction to Case $T_C=85^{\circ}\text{C}, T_J=200^{\circ}\text{C}, \text{DC test}$	$R_{\theta JC}$	0.35	$^{\circ}\text{C/W}$
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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Breakdown Voltage ($V_{GS}=0\text{V}; I_D=100\mu\text{A}$)	V_{DSS}	75			V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28 \text{ V}, V_{GS} = 0 \text{ V}$)	I_{DSS}			1	μA
Gate--Source Leakage Current ($V_{GS} = 6 \text{ V}, V_{DS} = 0 \text{ V}$)	I_{GSS}			1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}, I_D = 1 \text{ mA}$)	$V_{GS(th)}$		2.2		V
Gate Quiescent Voltage ($V_{DD} = 28 \text{ V}, I_{DQ} = 120 \text{ mA}, \text{Measured in Functional Test}$)	$V_{GS(Q)}$		2.74		V

Functional Tests (In Innogrator Test Fixture, 50 ohm system) : $V_{DD} = 28 \text{ Vdc}, I_{DQ} = 120\text{mA}, f = 1300 \text{ MHz}, \text{CW Signal Measurements. Pin}=6\text{W}$

Output Power	P_{out}		250		W
Power Gain	G_p		16		dB
Drain Efficiency@Pout	η_D		60		%
Input Return Loss	IRL		-7		dB

Load Mismatch (In Innogrator Test Fixture, 50 ohm system): $V_{DD} = 28 \text{ Vdc}, I_{DQ} = 130 \text{ mA}, f = 1300 \text{ MHz}$

VSWR 10:1 at 250W pulse CW Output Power	No Device Degradation
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Figure 1: Picture of application fixture

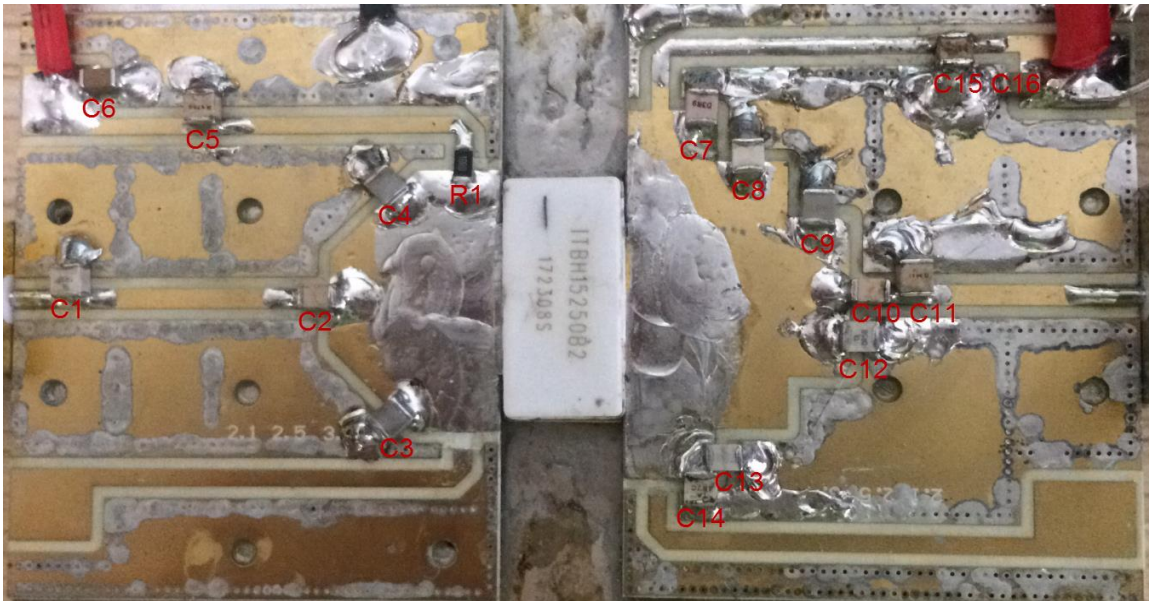


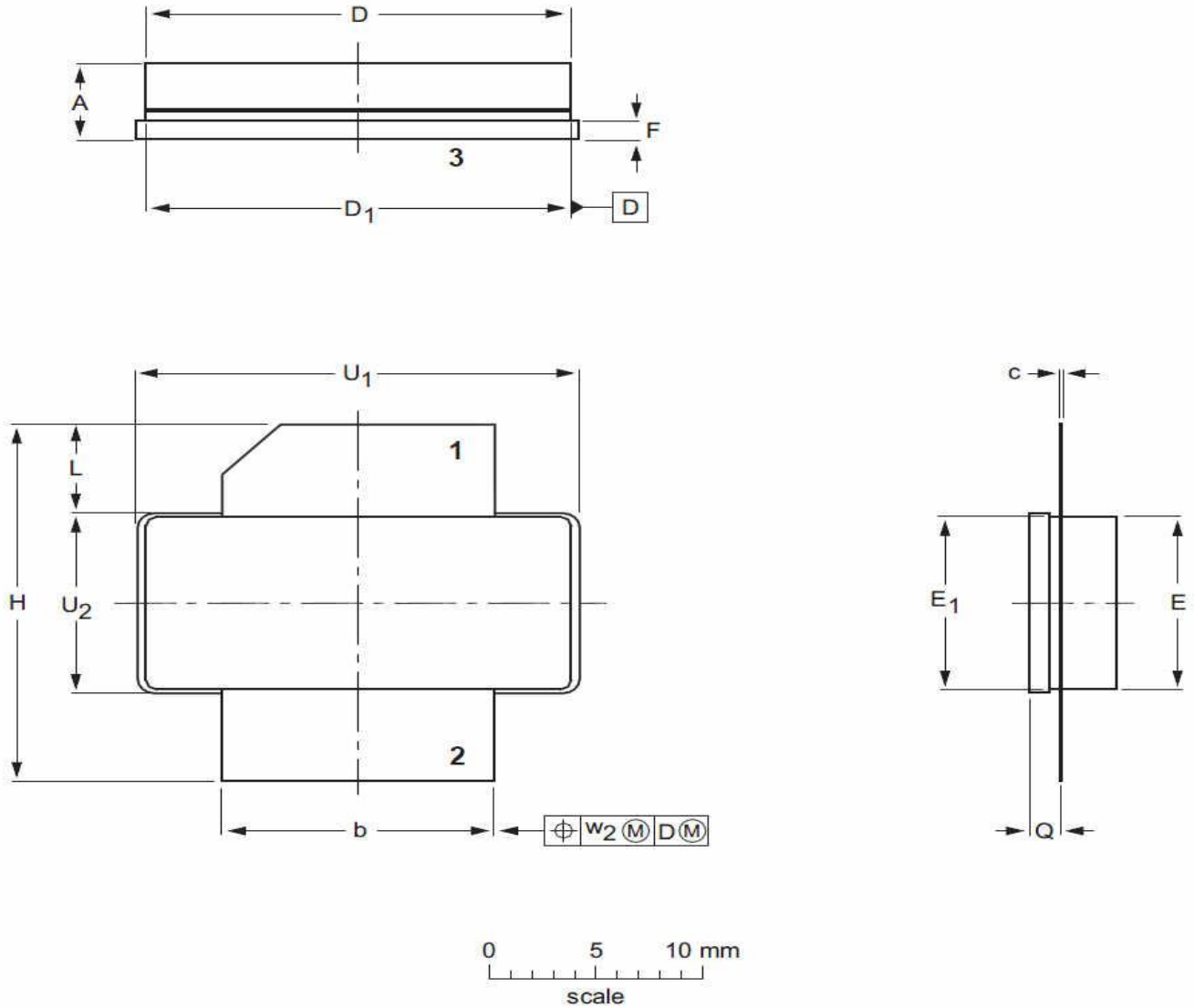
Table 5: Bill of Materials

C1,C8,C13	1PF	ATC100B
C2,C5,C10,C15	47PF	ATC100B
C3,C4,C14	4.7PF	ATC800B
C7	3.9PF	ATC100B
C9	1.8PF	ATC800B
C11	3.3PF	ATC100B
C12	0.5PF	ATC100B
C6,C16	1UF	1UF/50V
R1	10Ω	1206



Package Outline

Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2017/08/4	Rev 1.0	Production Datasheet

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